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طراحی و تحلیل نیم-جمع کننده پلاسمونی مبتنی بر موجبر فلزی از نوع اسلات

حامد رضوی خسروشاهی، حامد باغبان

دانشکده مهندسی فناوری‌های نوین، دانشگاه تبریز

چکیده – در این مقاله معماری یک نیم-جمع کننده پلاسمونی در ابعاد نانو به عنوان یک پردازنده ساده معرفی و مورد بررسی قرار گرفته است. بر اساس تداخل مد های پلاریتون های پلاسمونی سطحی در طراحی موجبرهای پلاسمونی از نوع اسلات، نشان داده شده است که عملیات منطقی ***XOR*** و ***AND*** را می توان با استفاده از پیکربندی موجبر دو شاخه و سه شاخه به دست آورد. طول انتشار قابل توجه 31.5 میکرومتر از چنین ساختار طراحی شده ای حاصل شده است.

کلید واژه- نیم-جمع کننده پلاسمونی، موجبر از نوع اسلات، طول انتشار

Design and Analysis of Plasmonic Half-Adder Based on Metal Slot Waveguide

Hamed Razavi Khosroshahi, Hamed Baghban

School of Engineering-Emerging Technologies, University of Tabriz, Tabriz, Iran

Abstract– *A nanoscale plasmonic half-adder architecture as a simple plasmonic processor has been introduced and verified in this article. Based on interference of surface plasmon polariton (SPP) modes in properly designed plasmonic slot waveguides it has been shown that logical XOR and AND operations can be demonstrated using two- and three-branch waveguide configurations. A considerable propagation length of ~31.5 μm has been obtained for the designed structure.*

Keywords: *plasmonic half-adder, slot waveguide, propagation length*

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Design and Analysis of Plasmonic Half-Adder Based on Metal Slot Waveguide

Hamed Razavi Khosroshahi

hamed.razavi91@ms.tabrizu.ac.ir

Hamed Baghban

h-baghban@tabrizu.ac.ir

1 Introduction

Based on high-speed and low heat production by photonic devices, these elements are promising for replacing the semiconductor-based optoelectronic devices and circuits [1]. For decades, optoelectronics have proved to be the best solution for transmitting data from one point to another, as can clearly be seen by the growth of the massive fiber optics communications industry [2]. It is important to scale down photonic devices further to realize direct integration with solid-state chips. Surface plasmon polaritons, which are localized surface electromagnetic waves at the interface of metal and dielectric, can be utilized to overcome this problem. However, due to subwavelength features of plasmonic devices, optical computing and ultrahigh speed information processing using optical plasmonic logic gates has attracted enormous attention in recent years. The main idea in this field is to control the constructive/destructive interference of two light signals in two or more plasmonic slot waveguides [3]. Plasmonic logic gates such as OR, AND, XOR, XNOR and NOT logical operations can make the elementary units of future sub-wavelength processors. Until now, only a few experimental results have been reported [3].

A few studies have been reported about plasmonic logic gates. In a study Yulan Fu et al [3] an experimental demonstration of logic gates has been presented the logic gates using plasmonic slot waveguides. Also, a theoretical study on AND, OR and XNOR logic gates and the analysis of different input and the outputs have been performed in [1].

In this paper, we propose a plasmonic half-adder structure as a simple processor based on plasmonic XOR and AND gates formed by metal slot waveguides. A cosine-shaped waveguide structure can work as AND and XOR logic gates. We will show that a three-branch configuration can serve as AND logical gate with the third port as control input. The truth table of designed half-adder will be verified and the propagation length of the SPPs will be reported.

2 Design and Analysis

Figure 1 illustrates the cross section of a plasmonic slot waveguide along with the result for mode analysis for fundamental plasmonic mode.

The structure consists of a SiO_2 substrate with a thin Au film on substrate with a 100nm slot etched in the gold thin film. It is expected that the guided mode mostly is confined at the interface of metal and dielectric. As it is shown in Figure 1 (b), a very good field confinement is accessible with such configuration which can be evaluated using the calculated effective mode index at operation wavelength of 530nm. The obtained effective index for fundamental plasmonic mode is $n_{eff} = n_{re} - in_{im}$ = 1.727683-0.015784i which implies a propagation length equal to 31.49 μm using the following relation [4]

$$Lp = \frac{1}{2 \times n_{im}} \qquad (1)$$

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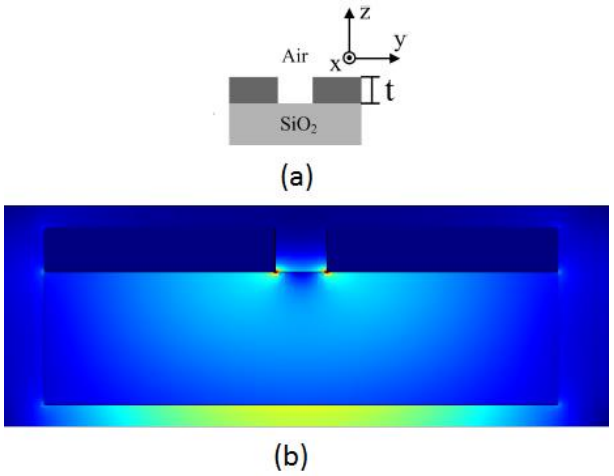


Figure 1: (a) Schematic of a simple slot waveguide. (b) The mode analysis of slot waveguide.

The derived value for propagation length in comparison to other plasmonic waveguides is much better. 11um propagating length in first models of waveguides shows that the introduced structure has an improvement in this parameter. [3] A logical half-adder structure can be demonstrated based on one XOR and one AND gate. With a symmetric Y-shaped or cosine-shaped slot waveguide we have designed AND logic gate in a 3 branch architecture where the 3rd branch acts as a control port to manage the output. Figure 2 depicts the sketch of designed half-adder structure using the plasmonic slot waveguides with related input (A, B and AvB) and output (S and C) ports.

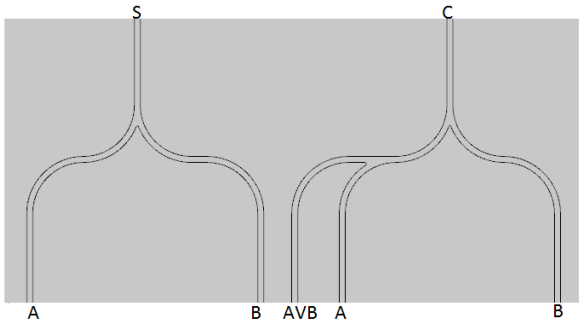


Figure 2. Sketch of a half adder based on slots in Au film

3 Results and Discussion

According to the truth table for the half adder, as shown in Table 1, we excite the input ports of the half-adder in different modes to have the sum and carry outputs.

In the simulation, we apply two different powers for input '1' and '0' logics. For '0' logic the input ports are excited with a very weak power, under P_0 (P_0 is threshold power), and for '1' logic the excitation power has been considered to be over P_0.

Input		Output	
A	B	S	C
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Table 1. The truth table of a half-adder

Figure 3(a) shows the obtained results for input logical values of '0'-'0' where output values of S= '0' and C= '0' have been obtained. It should be noted that the power intensity shown in the simulation result for output C does not implies to logic '1' since the output power is under P_0. For input logics of '1'-'0' and also, for both inputs at '1' logic, the result have been illustrated in Figure 3(b) and 3(c), respectively.

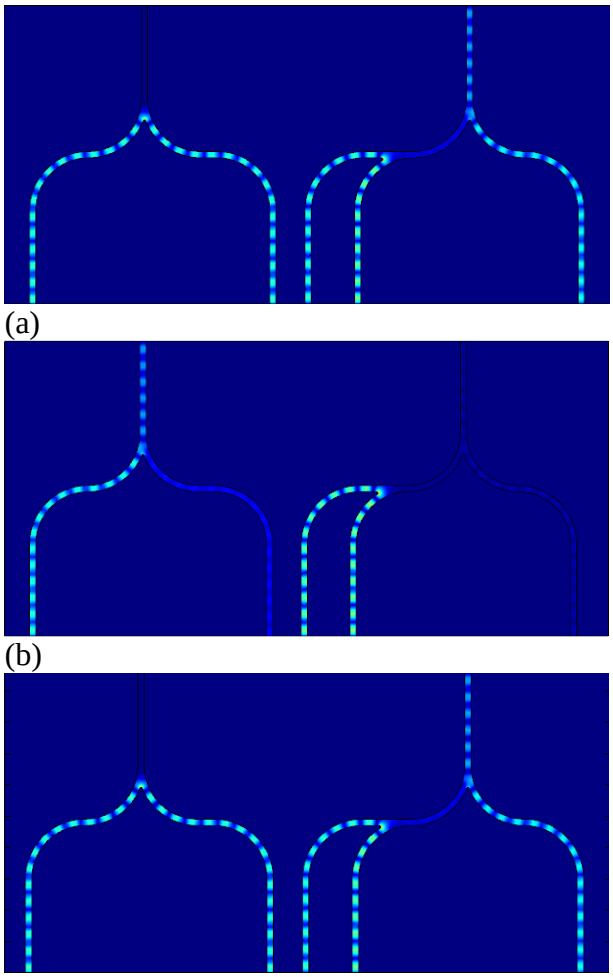


Figure 3. The simulation results of designed half-adder (a) 0-0 inputs resulted in 0-0 outputs, (b) 1-0 inputs resulted in 1-0 outputs, (c) 1-1 inputs resulted in 0-1 outputs.

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4 Conclusion

A plasmonic half-adder using designed XOR and AND logic gates was demonstrated. Interference of SPP modes in plasmonic slot waveguides based on Au film and air gap can be utilized to design variety of sub-wavelength logic gates. Simulations of in this study were performed using the finite element method in COMSOL software.
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